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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,402	12/04/2003	Kenneth J. Eldredge	200209367-1	7703

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,402	ELDREDGE ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12 and 18-20* is/are rejected.

7)☒ Claim(s) *7 and 13-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-6, 8, 11-12 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yatabe (US PAT No. 6,636,071).

Regarding claim 1, Fig. 1 of Yatabe teaches a method for translating voltage levels of digital signals (output voltage of 410), said method comprising: providing a first digital signal (output voltage of 410) operating between a first voltage (ground) and a second voltage (V1'), the first voltage corresponding to a logic 0 (ground) and the second voltage corresponding to a logic 1 (V1'); providing the first digital signal as an input to a capacitive element (500), an output of the capacitive element being electrically connected in parallel to a first branch (D1) and a second branch (D2), the first branch being electrically connected to a third voltage (V2), the second branch being electrically connected to a fourth voltage (V3); and causing the first and second voltages to interact with the first branch and the second branch such that a second digital signal

is produced (output of 610), the second digital signal operating between the third voltage and the fourth voltage (output of 610 is between V2 and V3).

Regarding claim 2, Fig. 1 of Yatabe teaches the method of claim 1, wherein the first voltage corresponds to ground, and the second voltage is approximately 5 V (col. 1, lines 36-38).

Regarding claim 4, Fig. 1 of Yatabe teaches the method of claim 1, wherein the third voltage and the fourth voltage exhibit an average value, the absolute value of which is at least an order of magnitude different than an average value of the first voltage and the second voltage (Fig. 2 shows the input and output where the absolute value of V2 and V3 are different from V1 and GND;col. 5, lines 5-15).

Regarding claims 5 and 11 Fig. 1 of Yatabe teaches a method or an apparatus for translating voltage levels of digital signals, said method comprising: providing a circuit board (placing a voltage translator on a circuit is the intended use of the voltage translator); providing, on the circuit board, a first digital signal (output signal of 410) operating between a first voltage (ground) and a second voltage (V1'), the first voltage corresponding to a logic 0 (ground) and the second voltage corresponding to a logic 1 (V1'); and providing, on the circuit board, a second digital signal (output of 410) operating between a third voltage (V2) and a fourth voltage (V3), the third voltage and the fourth voltage exhibiting an average value, wherein the average value has an

absolute value that is at least an order of magnitude different than an average value of the first voltage and the second voltage, the first voltage and the second voltage being used to produce the second digital signal (Fig. 2 shows the input and output where the absolute value of V2 and V3 are different from V1 and GND;col. 5, lines 5-15).

Regarding claims 6 and 12, Fig. 1 of Yatabe teaches the method of claim 5 and the apparatus of claim 11, further comprising: providing, on the circuit board, a capacitor (500) electrically connected between the first digital signal and the second digital signal, the capacitor being selected to prevent voltage levels associated with the second digital signal from altering the first digital signal (the capacitor 50 inherently isolates DC biasing between input and output, which will alter the input voltage).

Regarding claims 8 and 18, Fig. 1 of Yatabe teaches the method of claim 5 and the apparatus of claim 11 wherein the first voltage corresponds to ground, and the second voltage is approximately 5 V (col. 1, lines 36-38).

Claims 5, 8,10-11, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Orisaka et al. (US PAT No. 6,107,857).

Regarding claims 5 and 11 Figs. 17-18 of Orisaka et al. teaches a method or an apparatus for translating voltage levels of digital signals, said method comprising: providing a circuit board (placing a level conversion circuit on a circuit board is the intended use of the level conversion circuit); providing, on the circuit board, a first digital

signal (INPUT SIGNAL IN at T1) operating between a first voltage (GND) and a second voltage (VLS; see Fig. 18A), the first voltage corresponding to a logic 0 (GND, "L") and the second voltage corresponding to a logic 1 (VLS, "H"); and providing, on the circuit board, a second digital signal (OUTPUT SIGNAL OUT at T2) operating between a third voltage (VCC) and a fourth voltage (VSS), the third voltage and the fourth voltage exhibiting an average value, wherein the average value has an absolute value that is at least an order of magnitude different than an average value of the first voltage and the second voltage, the first voltage and the second voltage being used to produce the second digital signal (Fig. 18A shows the input and output where the absolute value of VCC and VSS are different from VLS and GND).

Regarding claims 8 and 18, Figs. 17-18 of Orisaka et al. teaches the method of claim 5 and the apparatus of claim 11 wherein the first voltage corresponds to ground, and the second voltage is approximately 5 V (GND, and VLS between 3 - 5 volts).

Regarding claims 10 and 20 , Figs. 17-18 of Orisaka et al. teaches the method of claims 5 and 11, wherein a difference between the first voltage and the second voltage is approximately equal to a difference between the third voltage and the fourth voltage (Fig. 18B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yatabe and/or Orisaka et al. .

Regarding claims 3, 9 and 19, Yatabe and/or Orisaka et al. disclose the method/system according to claims 1, 5 and 11 as discussed above except the third voltage being approximately -695 V, and the fourth voltage being approximately -700 V. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the third voltage being approximately -695 V, and the fourth voltage being approximately -700 V, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Allowable Subject Matter

Claims 7 and 13-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Yatabe and Orisaka et al. teaches a level conversion circuit, one of ordinary skill in the art would not have been motivated to modify the teaching of Yatabe and/or Orisaka et al. to further includes, among other things, the specific of the first branch including a first diode and a first RC circuit electrically connected in parallel between a source of the third voltage and the capacitor, the second branch including a

second diode and a second RC circuit electrically connected in parallel between a source of the fourth voltage and the capacitor as set forth in claims 7 and 13.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shokouhi (US PAT No. 6,369,612) discloses a high voltage level-shifter with tri-state output driver.

Sasaki et al. (US PAT No. 6,522,323) discloses a level shift circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

7-6-2005